



UNITED STATES PATENT AND TRADEMARK OFFICE

cen
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,253	06/16/2006	Eiji Yamamoto	Q95326	9117
23373	7590	11/19/2007		
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER DIAO, M BAYE	
			ART UNIT 2838	PAPER NUMBER
			MAIL DATE 11/19/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/583,253	Applicant(s) YAMAMOTO ET AL.	
	Examiner M'baye Diao	Art Unit 2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 June 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>06/16/2006</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed on 06/16/2006 has been considered and placed of record. An initialed copy is attached herewith.

Specification

3. The disclosure should be carefully reviewed to ensure that any and all grammatical, idiomatic, and spelling or other minor errors are corrected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1- 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Sawa et al., (Sawa) US PAT 6,351,397.**

6. As per claims 1 - 4, Sawa discloses (abstract; col. 2, lines 35+; col. 5, lines 29+; cols. 6 -7; col.8, lines 1-60) and show in Figs. 1 - 6:
an input voltage detection apparatus, for a PWM
cycloconverter that is a power converter wherein individual
phases (r or s or t) of three-phase AC power (1) are directly connected (via switches (3)

to (20)) to

individual phases (u,v,w) of a three-phase output of the power converter by employing a bidirectional semiconductor switch ((3 and 4),(5 and 6),(7 and 8),(9 and 10)....(19 and 20), see Figs. 1, and 6-7) that is formed by combining two unidirectional semiconductor switches (for example (3) and (4)), to which a current is supplied only in one direction (because of the series connected diodes) and which are capable of independently being turned on and off (since the unidirectional semiconductor switches are connected in parallel, also see col. 2, lines 44-55), the input voltage detection apparatus comprising: an input power voltage phase detector (30), for detecting a phase of the three-phase AC power (1); an artificial DC bus voltage detector (22), for employing the three-phase AC power (1) and the phase detected by the input power voltage phase detector (30) to detect an artificial DC bus voltage (50) that represents a magnitude of the three-phase AC power (1) as a difference between a maximum value (V_p) and a minimum value (V_n) (via the gate signal combining section (24), see col. 6, lines); an ideal input voltage calculator (24), for calculating an ideal input voltage value (V_m) based on an effective value of the artificial bus voltage (50) and the phase of the input voltage (detected by input voltage information detection system); an input voltage upper and lower limit calculator (24) (since the gate signal combining section outputs the result of Oring $G_{1xy}, G_{1yyx}, G_{2xy}, G_{2yx}$ as G_{xy}, G_{yx} , see Fig. 4), for calculating a permissible width (permissible being $V_p - V_n$) defined by upper (V_p) and lower (V_n) limits for the obtained ideal input voltage value (V_m); and a voltage comparator (117), for comparing a voltage value detected by the pseudo DC

bus voltage detector with the permissible width (V_p - V_n) defined by the upper (V_p) and lower (V_n) limits, which are obtained by the input voltage upper and lower limit calculator (24),

wherein an output of the voltage comparator (117)(see Fig. 5) is adjusted, so that a voltage value (V_m) detected (which falls within the lower (V_n) and upper (V_p) limits)by the artificial DC bus (50)(since the protection switching means (50) is responsive for turning on and off the unidirectional semiconductor switches of the PWM cycloconverter based on the fault signal output from the detection means whenever a fault signal occurs, see abstract) voltage detector falls within the permissible width defined by the upper (V_p) and lower (V_n) limits, which are obtained by the input voltage upper (V_p) and lower (V_n) limit calculator (24) (claims 2 & 4).

Accordingly, claims 1 - 4 are anticipated.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in the PTO-892 and not mentioned above disclose related apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M'baye Diao whose telephone number is 571-272-9748. The examiner can normally be reached on 8:30-5:00; First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on Monday through Thursday at 571-272-2361.

Application/Control Number:
10/583,253
Art Unit: 2838


Page 5

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

M'baye Diao
Examiner
Art Unit 2838

M.D



BAO Q. VU
PRIMARY EXAMINER